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A sampled spur free fractional frequency synthesizer and its noise analysis

Marc Houdebine, Sébastien Dedieu

ST Microelectronics Crolles,

850 rue Jean Monnet,

38926 Crolles Cedex, FRANCE

Email: {Marc.Houdebine, Sebastien.Dedieu}@st.com

Olivier Sename, Mazen Alamir

Laboratoire d'Automatique de Grenoble,

UMR CNRS-INPG-UJF 5528, ENSIEG-BP 46,

38402 Saint Martin d'Hères Cedex, FRANCE.

Email: {Olivier.Sename, Mazen.Alamir}@inpg.fr

Abstract—This paper presents a new fractional frequency synthesizer architecture and its noise analysis model. The proposed analysis model takes into account the sampled behavior of the PLL. In order to validate this study, measurement results illustrate the output frequency purity and the reliability of the model.

I. INTRODUCTION

Widely used in modern electronics, local oscillators are based on Phase Locked Loop architectures (PLL) by locking a tunable oscillator (VCO) to an accurate frequency source as a crystal oscillator. This reference clock gives rhythm to the Voltage Controlled Oscillator (VCO) input voltage refreshing and induces parasitic rays to the output phase noise spectrum. Because the frequency spacing between these parasitic rays called “spurious” and the carrier frequency is equal to the reference clock frequency, the reference clock is chosen as high as possible. Moreover, by increasing the reference clock frequency, the loop bandwidth can be larger which decreases the settling time. Another benefit is the output-reference frequency ratio diminishing which reduces the output noise contribution of the reference clock. All these advantages induce to increase the reference clock frequency as high as possible, but to meet the output frequency step lower than the reference frequency value, the output-reference frequency ratio have to be real and not only integer.

Because low noise frequency dividers are comparable to counters, they can only make integer division. To make fractional division, classical PLLs uses several dividers on the feedback path switched according to the desired fractional frequency ratio degrading the output spectra purity by adding other spurious tones due to “quantization noise” [1].

The structure presented in this paper is a spuriousless fractional RF frequency synthesizer taking advantages of a sampled working to get free of the limiting quantization noise.

To study the noise performances of the loop, linear continuous models are mostly used providing a loop bandwidth much below than the sampling frequency fixed by the reference clock [2]. Some models consider the sampling as a delay [3], [5]. It has also been presented a mixed z - s model in [4] close to classical models. In this work, we propose an appropriate discrete time model taking the switch aperture time into account.

The content of this paper is as follows. The proposed spur free fractional frequency synthesizer architecture is presented in section II. Section III develops the appropriate noise model taking the sampled behavior into account. Some measurement results are depicted in section IV.

II. THE SPUR FREE FRACTIONAL FREQUENCY SYNTHESIZER

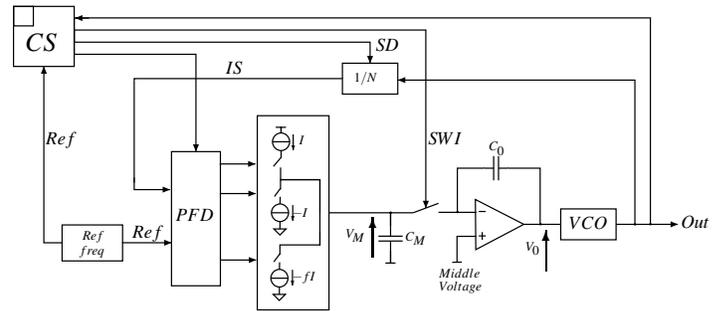


Fig. 1. The Spur free Fractional Frequency Synthesizer architecture

The proposed fractional frequency synthesizer architecture is shown in Fig. 1. The removal of quantization noise is due to the system working by two time cycles: first the output frequency measurement followed by the VCO input control voltage correction. During the output frequency measurement, charges are injected into the measurement capacitor V_M . In order to avoid disturbing the output frequency during the measurement, the signal SWI opens the switch to isolate the VCO from the measurement capacitor C_M . The VCO input control voltage V_0 is kept constant by the capacitor C_0 . As shown in Fig. 2, when the output frequency measurement is done, the phase displacement between the reference clock and the output is memorized into capacitor C_M . The input voltage correction is then possible by closing the switch starting the charge transfer from capacitor C_M to C_0 .

A. The output measurement method

Let N be the integer part of the frequency ratio and f the corresponding fractional part:

$$F_{out} = (N + f)F_{ref} \quad \begin{cases} N \in \mathbb{N}. \\ 0 \leq f \leq 1. \end{cases} \quad (1)$$

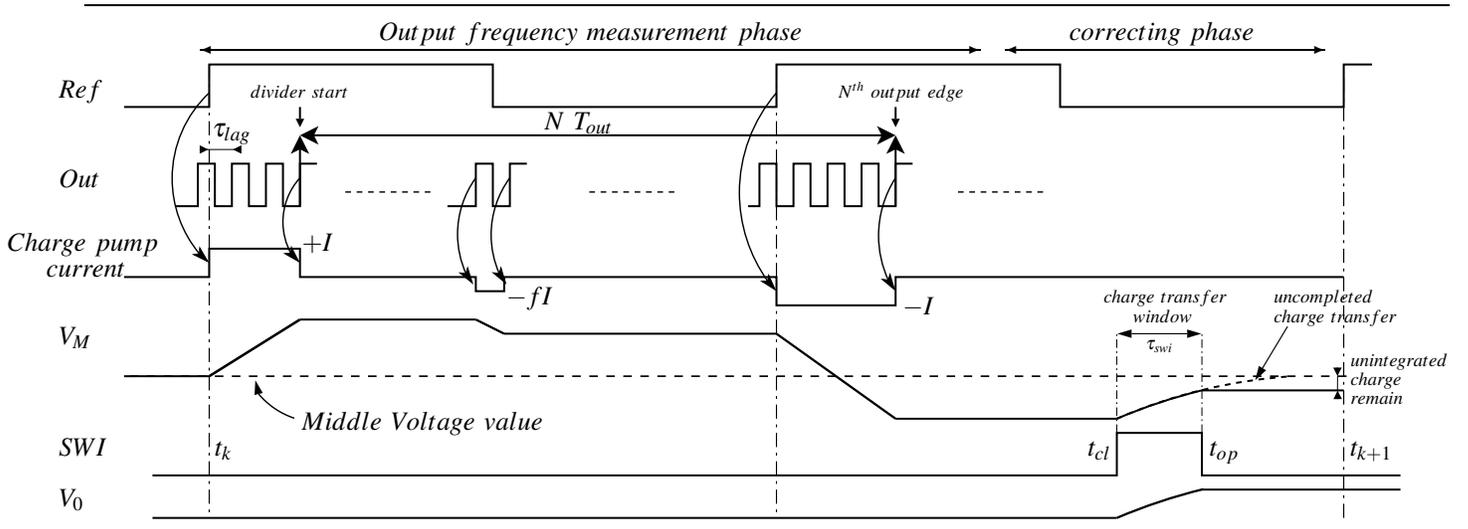


Fig. 2. Chronogram of the sampled Frequency Synthesizer architecture in an unlocked case.

When the system is locked, a cyclic phase displacement τ_{lag} is due to the fractional part since $T_{ref} = (N + f)T_{out}$. In order to be insensitive to this natural phase displacement, two opposite currents are injected from the reference phase to the output phase. To avoid any dead zone, the first current is injected for more than 2 output periods. The last current injection will stop at the N^{th} output rising edge from the divider start (see Fig.2). The fractional part is added to these currents during one output period and in the end of measurement, charges stored in a lock case are equal to:

$$\Delta Q = (\tau_{lag} + 2T_{out})I - fIT_{out} - I(\tau_{lag} + (1 - f)T_{out} + T_{out}) = 0.$$

B. The correcting charge transfer

In Fig.2, an unlocked case is voluntarily shown in order to illustrate the charge transfer through the switch window. As detailed in Fig.3, the resistor R makes possible the loop bandwidth setting. On the other hand, the charge transfer is slowed down. For practical reasons, this resistor is placed before the switch in order to have a small contribution to the PLL output noise. For noise reduction, the amplifier is reduced to a simple MOS and the Middle Voltage is fixed by its V_{gs} . This Middle Voltage corresponds to the mean value of the measurement voltage V_M at the charge pump output. Because charge pump sink and source currents are

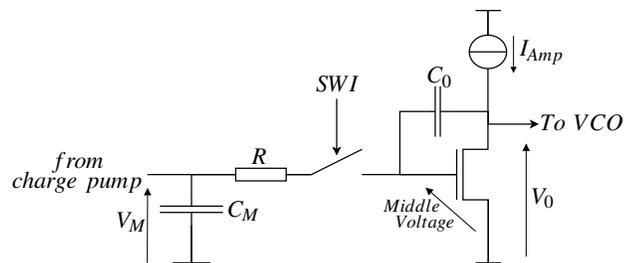


Fig. 3. Charge transfert circuit details

best equivalent ($|+I| = |-I|$) when its output bias voltage is kept close to half the supply voltage, the MOS transistor is dimensioned to set its V_{gs} at half the supply voltage.

So, for whole charge transfer, V_M comes back to its mean value. But when it is not the case as shown in Fig.2, some charges remain in C_M and will have to be discharged for the next time added to the next accumulated measurement charges.

This bring us to the necessity of an appropriate noise model. For more details, please see [6], and for further information about the system nonlinearity, see [7].

III. AN APPROPRIATE MODEL TO SAMPLE DATA SYSTEMS

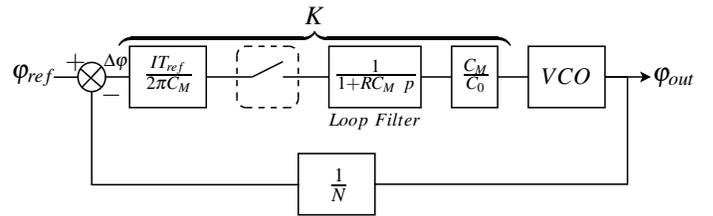


Fig. 4. Small signal Model establishing

As shown in the previous section, the switch window has to be considered in small signal models.

Because the voltage V_0 is kept constant by capacitors C_0 when the switch is open (see Fig.2), its value at the switch closing instant t_{cl} is equal to its value at instant t_k . Then, at the switch opening instant t_{op} , its value doesn't change until the instant t_{k+1} . In view of this, we can consider only the instant t_k and t_{k+1} .

As well as for V_0 , the value of V_M doesn't change from instant t_{op} to the instant t_{k+1} . Because the measurement charges are injected into C_M while the switch is open, regarding from V_0 , V_M value has changed instantaneously at the instant t_k .

In fine, at the sight of the VCO control voltage, instant t_k and t_{k+1} can be considered as respectively the switch opening

and closing instant, and the sampling period is equivalent to the closed switch window τ_{swi} . On the other hand, during the switch opening, the charge pump current is integrated for the time difference $\Delta t = \Delta\phi \frac{T_{ref}}{2\pi}$ and V_M results from these charges integration into C_M :

$$V_M = \frac{IT_{ref}}{2\pi C_M} \Delta\phi \quad (2)$$

Then, the expression of K (Fig. 4) can be found by the exact discretization method [8]:

$$K(z) = \frac{IT_{ref}}{2\pi C_M} \frac{C_M}{C_0} (1-z^{-1}) \mathcal{Z} \left\{ \mathcal{L}^{-1} \left[\frac{1}{s(1+RC_M s)} \right] \Big|_{\tau_{swi}} \right\} \quad (3)$$

Because the MOS grid (Fig. 3) voltage doesn't significantly change, the effective components involved in the filtering are only R and C_M . Charges are then transferred from C_M to C_0 such that the charge conservation implies: $Q = C_M V_M = C_0 V_0$. Equation (3) leads to:

$$K(z) = \frac{IT_{ref}}{2\pi C_0} \left(\frac{1 - e^{-\frac{\tau_{swi}}{RC_M}}}{z - e^{-\frac{\tau_{swi}}{RC_M}}} \right) \quad (4)$$

Likewise, the equivalent VCO discrete time model is:

$$G(z) = 2\pi K_o \frac{2T_{ref}}{z-1} \quad (5)$$

It is worth noting that the presented frequency synthesizer only needs one divider on the feedback path such that the corresponding model is a simple gain equal to the opposite of the frequency ratio integer part.

This approach which takes the switch opening and closing time into account will now be compared with measurement results.

IV. MEASUREMENT RESULTS

A fully integrated test chip was designed in technology CMOS 120nm. The circuit layout uses the 6 metal levels and capacitors C_M and C_0 are Metal On Metal capacitors (MOM) from metal 2 to metal 5, no specific option as inter metal thin

VCO	0.211mm ²
control loop	0.162mm ²
Total	0.39mm ²

a. Silicon Area

F_{ref}	27MHz
F_{out}	1.2GHz - 1.75GHz
τ_{swi}	1.5ns

c. Time/Frequency values

VCO+buffer	48.5mA
Analog part	3.1mA
Digital part	1.4mA
Total	53mA

b. Current consumption

R	20k Ω
C_M	20pF
C_0	20pF
K_0	100MHz/V
I_{chpp}	200 μ A

d. parameter values

TABLE I
PLL CHARACTERISTICS

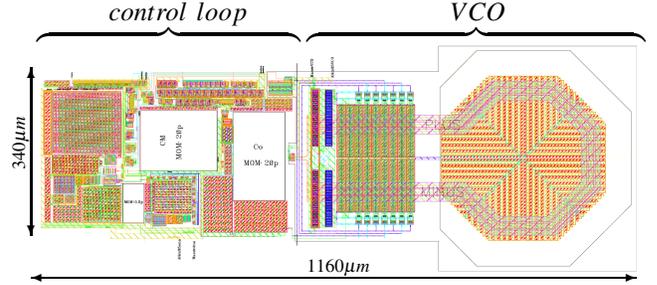


Fig. 5. view of circuit layout

oxide capacitor (MIM) was used. The circuit characteristics are reported in table I. The output frequency range is from 1.2GHz to 1.75GHz by 210kHz steps. The reference quartz frequency is 27MHz.

As we can see in Fig. 6, there are still one unavoidable spur owing to the VCO tuning node refreshing at each sampled time. The reference frequency is chosen as high as possible to decrease the sample time in order to push aside these spurs from the carrier. Because two reference clock periods are needed to execute one sample time, the carry-spur spacing is equal to $F_{ref}/2 = 13.5MHz$. Added to these spurs, additional

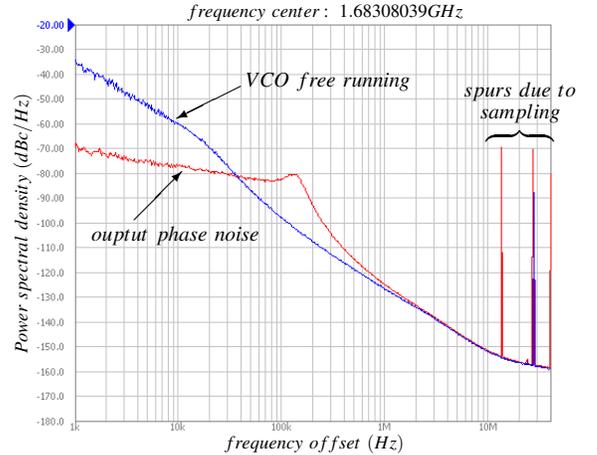


Fig. 6. output Phase Noise measurement (Agilent E5052A)

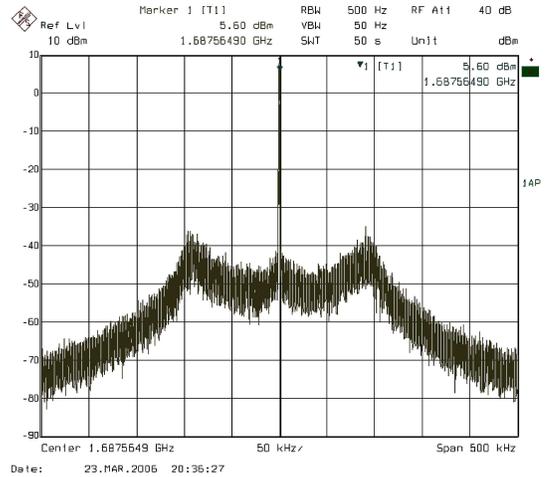


Fig. 7. Spectrum analyser measurement

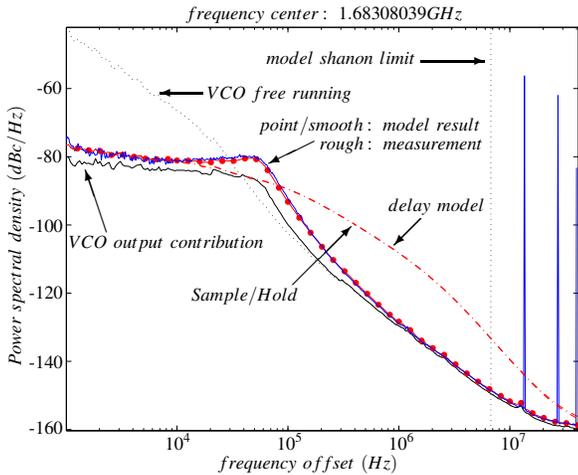


Fig. 8. model/measurement corroboration with $I_{chpp} = 50\mu A$

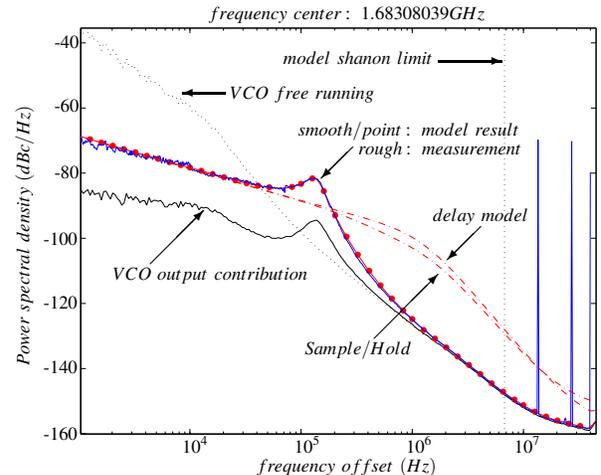


Fig. 9. model/measurement corroboration with $I_{chpp} = 200\mu A$

rays are due to clock feedthrough of the sampling switch. Indeed, because the switch is a MOS transistor, when its grid command SWI changes, its parasitic capacitors values changes inducing a small parasitic charge injection. This charges injected or suppressed at instants t_{cl} and t_{op} are integrated in C_0 and creates periodic disturbances at the VCO input control voltage as detailed in [4]. As shown in [4], the worst case on the switch opening command SWI is a 50% duty cycle.

Fig. 6 shows the PLL output phase noise measured with the Agilent E5052A signal source analyser. It represents the offset frequency from the carrier shown in Fig. 7. The center frequency is such that the output-reference frequency ratio is equal to: $N + f = 62.336$. Spurs due to the sampling clearly appear at one (13.5MHz), at twice (27MHz) and three times (40.5MHz) the sampled frequency. In spite of these well known and unavoidable spurs, there is no added spurious due to the fractional part.

Fig. 8 and 9 show the presented model result overwritten on measurement results with a charge pump current of respectively $50\mu A$ and $200\mu A$. Dashed-dotted lines also show the output noise calculated by considering the sampling as a delay $e^{-2T_{ref}s}$ (delay model) or by establishing a sampled and hold model with a frequency sampling at $2T_{ref}$. Our model is more suitable because it takes the switch opening and closing time into account especially when the closing time is much lower than the opening time.

The model shanon limit shown in dashed line on Fig. 8 and 9 represents the model maximum frequency validity. Because this frequency at half the sampling period is much larger than the PLL bandwidth, no noise information is hidden. Indeed, as it is clearly shown, the VCO output noise contribution is high-pass filtered by the loop. For frequencies over 1MHz, the VCO is the main output contributor. So, over the model shanon limit, the PLL output phase noise is equal to the VCO phase noise.

This test chip target was to validate this new PLL architecture and its study, so the circuit performances were not optimum but it will be so in the next circuit.

V. CONCLUSION

A fully integrated on silicon RF frequency synthesizer has been presented. It has been demonstrated that the sampled working is the solution to avoid any fractional spur.

Because the switch aperture is much lower than the reference clock period, classical continuous models are ineffective for noise analysis. Then, a discrete time model was established to study this PLL output phase noise profile. The sampled model reliability as well as this new PLL architecture has been validated with a chip demonstrator.

VI. ACKNOWLEDGMENTS

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