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VHDL simulation of Magnetic Domain Wall Logic

Jacques-Olivier Klein, Eric Belhaire, Claude Chappert,
Russel P. Cowburn, Dorothee Petit, and Dan Read

Abstract—The VHDL simulation of domain wall logic allows to validate magnetic circuits functionality early in the design stage. In this paper, we present two VHDL simulation techniques for domain wall logic. The first one, closer to the physics, uses models of components described at the behavioral level. It allows to study the basic functions and reveals the specificities of DW logic. The second one, closer to the logic, models components with logic gates and delays and it allows very fast simulation of complex circuits.

Index Terms—Magnetic logic devices, Digital simulation, Circuit simulation

I. INTRODUCTION

THE exponential growth of digital circuit complexity requires to automate their design flows. Automatic synthesis tools and hardware description language such as VHDL [1] allow nowadays to rapidly design very complex circuits containing thousands or even millions of transistors. At each step of the design flow, comparative simulations ensure the coherency among the various views, from the most abstract to the most physical. We have applied this approach to the magnetic domain wall logic (MDWL), building on the recently demonstrated set of basic logic gates [2-3]. The cell size depends on the particular gate, but typically gates are between $10\text{-}20 f^2$, if f is the minimum feature size, here the width of the ferromagnetic thin film line. The various logic gates fabricated have been tested over a minimum of 100,000 clock cycles. This proves that the successful operation rate of the different elements is higher than 99.99999% for a given chip. Although, no experimental measurements has been made with very high clock speeds, such logic structures are expected to operate up to 100 MHz. This can be inferred from measurements which showed DW velocities in Permalloy nanowires to be of the order of 500m/s [4].

In this paper, we present two VHDL simulation methodologies for MDWL. Section II summarizes the specificities of magnetic logic circuit. Then, section III focuses

on a first simulation technique based on behavioral models. Finally, the analysis of simulation results in section IV leads to the functional simulation described in section V.

II. DOMAIN WALL LOGIC

Magnetic domain walls (DW) can propagate in nanowires (NW) when helped by an externally applied magnetic field. In addition, they can split when they meet a “Y-shape” fork and turn in 90° -bends with a rotating field. We will note T the period of the rotating field. Moreover, as DW follow the rotation direction of the rotating field, we can define a propagation direction along the NW. This one is used to define the logic levels. Arbitrarily, the HIGH logic level '1' (resp. LOW and "0") is associated to a magnetization directed along (resp. against) the direction of signal propagation. Furthermore, at the expense of a $T/2$ -delay cusp-shape NOT gates [2], can complement the logic state of a magnetic signal. Finally, “Y-shape” logic gates have been demonstrated. They require an elliptic rotating field with a DC offset [3]. Depending on this DC offset, the same 2-input gate can behave as an AND or an OR gate. For example, with a negative DC offset (towards the left), gates directed in the propagation direction of the positive signal (towards the right-hand side) will be AND gates while gates directed in the negative direction (towards the left) will be OR gates (Fig. 1). To operate the two kinds of logic gates on the same circuit and with the same global external field, both kinds of gates should be directed with opposite directions. As a consequence, the output of one kind of gates can be connected to the input of the other one only after a U-turn of the NW, that is, after two 90° -bends and a $T/2$ -phase delay (Fig. 1).

FIG. 1 HERE

Theoretically, the existence of AND gates and NOT gates is sufficient for building any logical function. Nevertheless, MDWL presents specificities that are unknown for CMOS electronic architectures. Especially, the signal propagation depends on its value: when the external rotating field is directed against the propagation direction it favors the propagation of '0's and other times the propagation of '1's. Consequently, functions and circuits synthesized using standard electronic methods should be validated using VHDL simulation of MDWL.

III. BEHAVIORAL SIMULATION

A structural description is first needed to allow simulation

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and validation of basic circuits. Starting from the operation principle of reference [3], the direction of the external magnetic field is coded with an integer in the range 0 to 7, generated by a modulo-8 counter. Its magnitude is a tabulated real function of the direction. Both direction and magnitude are distributed to all the components as VHDL signals.

FIG. 2 HERE

Four basic logic elements are then modeled: a 90°-bend, a NOT gate, a fan-out and a 2-input gate [3]. The elements are decomposed into sections, each characterized by an orientation coded with an integer in the range 0 to 7 and by switching thresholds (Fig. 2 and Fig. 3). In sections with only two neighbors, a DW, if it exists, will propagate only if the initial magnetization is set against the direction of the external field and if the field magnitude is greater than a "standard" threshold value. In 2-input-logic gates and fan-out elements, sections can have three neighbors: one of standard width (200 nm) and two narrower (125 nm). Such sections have three thresholds: the "standard" one for the propagation of a DW stemming from a normal section, a "high" one for the propagation of a DW stemming from a single narrow section and a "low" one for the fusion of two DW stemming from two narrow sections.

FIG. 3 HERE

As we already noted, such sections can be programmed as logic AND or logic OR gates, depending of the direction of a well chosen DC field offset added to the rotating field. In every section, the magnetization is coded with two VHDL internal states: one absolute and one relative. The absolute state is coded with an integer in the range 0 to 7, like an orientation, and allows detecting when the external magnetic field is set against the direction of magnetization. The second state is binary and relates to the direction of signal propagation imposed by the bends curvature and the direction of rotation of the magnetic field. Finally, except for the inner section of the NOT gate, a domain wall is considered existing when two connected sections have different relative orientations.

IV. SIMULATION RESULTS

Once described the four basic components, it remains only to instantiate and connect them in order to constitute the schematic view of the circuit (see Fig. 4). The simulation (Fig. 5) of MDWL circuits using this method reveals two specificities of magnetic components.

FIG. 4 HERE

FIG. 5 HERE

First, in "Y-shape" components signal can propagates backward. As 2-input gates and fan-out elements are symmetrical and share the same behavioral model, a 2-input gate can operate as a fan-out (and conversely). This case occurs when the two states of the gate inputs are not equal. In this situation, the absorbing element for the considered Boolean operator ('1' for OR gates and '0' for AND gates) forces the output state. Then, the gates operates like a fan-out

and the new output state back-propagates and reverse the state of the other input, that with the state equal the neutral element ('0' for OR gates and '1' for AND gates). Actually, this is not an insuperable drawback. Indeed, thanks to the rotation direction of the external field, the modified input state cannot back-propagates through a previous bend, nor it can back-propagate through fan-out because in this direction the absorbing element become the neutral element (Fig. 6).

FIG. 6 HERE

One crucial thing however is that straightforward synthesis of digital function, like counters or registers, using standard electronic method shows different simulation results between the electronic and the magnetic implementation. This is mostly due to the $T/2$ -delay associated with all NOT gates. This delay affects the synchronization of the input signals. As a consequence, signal must be actually synchronized and the external rotating magnetic field cannot be taken as a clock signal. Starting from this observation, we can assert that the delay inherent to logic functions constitute the main specificity of magnetic logic which forbids straightforward use of standard electronic synthesis methods.

V. FUNCTIONAL SIMULATION

This led us to develop a higher level functional data-flow description, more compact than a structural or schematic approach, where the propagation of the signal in a magnetic circuit is modeled with just basic operators and with half (=NOT gate) or quarter (=bend) period delays (Fig. 7). So, for instance, few lines are sufficient to describe a "magnetic counter". Synthesis and functional simulation of finite state machine will be published later.

FIG. 7 HERE

VI. CONCLUSION

We have presented two simulation techniques for magnetic domain wall logic. The first description, behavioral, reveals that the delays added to the logic operator in the case of magnetic implementation is the major drawback and forbids straightforward use of standard electronic synthesis methods. The second description, more compact, is functional and uses logic and delay elements. We are now building a synthesis library of basic logic functions along these lines.

REFERENCES

- [1] IEEE Standard VHDL Language Reference Manual, IEEE, New-York, 2000
- [2] D. A. Allwood, Gang Xiong, M. D. Cooke, C. C. Faulkner, D. Atkinson, N. Vernier, R. P. Cowburn, "Submicrometer Ferromagnetic NOT Gate and Shift Register" *Science*, Vol. 296. no. 5575, pp. 2003 – 2006, 14 June 2002
- [3] D. A. Allwood, G. Xiong, C. C. Faulkner, D. Atkinson, D. Petit, and R. P. Cowburn "Magnetic Domain-Wall Logic" *Science* vol. 309. no. 5741, pp. 1688 – 1692, 9 September 2005
- [4] Atkinson et al. *Nature Materials*, Vol 2, P85 2003

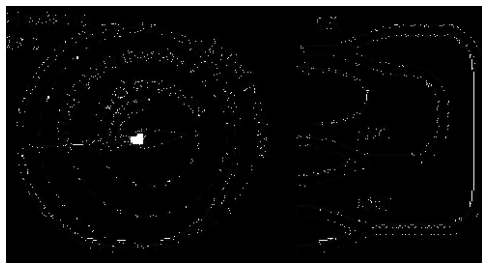


Fig. 1. The DC offset of the magnetic field indicates the OR or AND function of the 2-input gates. Here, the DC offset is negative (shifted to the left) helping domain of magnetization oriented to the left to propagate through fork-gates. As a consequence, gates with their output to the left (resp. right) are OR gates (resp. AND gates).

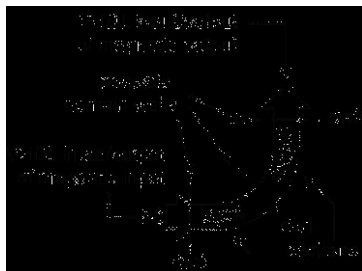


Fig. 2. Components are made of sections. A section is characterized by its physical orientation and its magnetization. DWs exist only on the borders of two sections with different magnetization. Both inputs and outputs of components contain a VHDL input signal and a VHDL output signal in order to detect the DW.



Fig. 3. A domain wall propagates through BEND, NOT and FANOUT components if helped by an external magnetic field greater than a STANDARD threshold. A domain wall propagates through 2-INPUT gates if helped by a HIGH threshold or two domain walls can fusion if helped by a LOW threshold.



Fig. 4. A magnetic domain wall circuit. The ring to the left generates the clock signal, and then the signal splits. One of the branches is complemented and delayed by a NOT gate N1 then both signals are combined in the final OR gate G1.

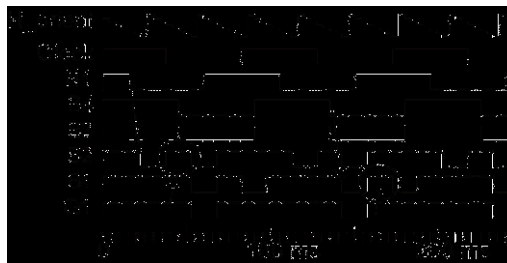


Fig. 5. Simulation result for the circuit presented figure 4. The output of the bend B2 does not follow exactly the output of gate N1 nor the output of bend B1 follows the output of bend B4: there is back-propagation of the signal '0' stemming from the output of G1.



Fig. 6. Forward / backward propagation in a complex logic circuit. Here, signal '0' stemming from A forces the output of the AND gates, until signal x. In addition, in the other direction AND gates behave as FANOUT components and the logic level '0' back-propagates and forces the others inputs of AND gates. Nevertheless, this back-propagation is limited on one side by the curvature of the bend after B and on the other side by the FANOUT element that behave is the reverse direction like an OR gate.

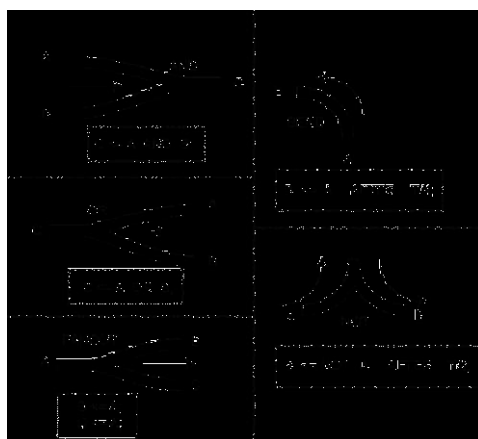


Fig. 7. Functional VHDL models using Boolean operators and delays.