

1-Min Decoding Algorithm of Regular and Irregular LDPC Codes

Frédéric Guilloud, Emmanuel Boutillon and Jean-Luc Danger





- - -

Problems of LDPC decoder architecture :

- > Memory cost of Check-to-Variable (Lmn) and Variable-to-check messages (Zmn).
- > Complexity of the Check Node Processor for irregular codes.

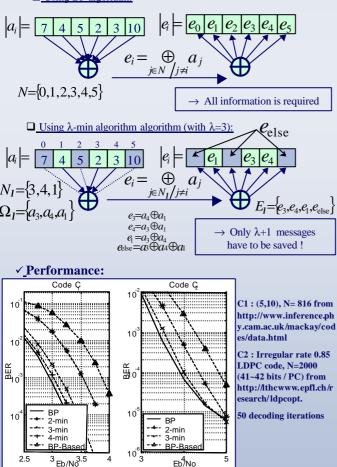
Solution: 1-Min Algorithm and its associated architecture

- □ Sub-optimal algorithm to compute Zmn values.
- Local storage of a compressed version of Lmn messages.
- □ Serial computation of check node, with on the fly computation of Zmn messages.

1-Min Algorithm:

- \checkmark Idea: Use the λ incoming messages which have the smallest magnitude, to compute extrinsic information.
- ✓ **Example:** a check node of degree 6 with λ =3 (signs are omitted)

Using BP algorithm:



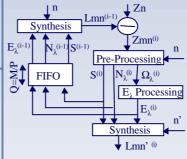
Note: the addition of a correcting factor (offset) in operation Å allows the 3-Min algorithm to over perform the BP algorithm

Architecture

Based on "decoder first code design" architecture (Boutillon et al., ISTC&RT'00)

 \Box P memory banks storing variables $Zn^{(i-1)}$ and processing $Zn^{(i)}$ by accumulation \Box P parity check processors working in parallel.

Shuffle (and unhsuffle) network between memory banks and PC processors.



Parity Check Processor

The M parity checks are processed by P parity check processors in C macro-cycle.

Each processor features 2 synthesis blocks and 1 pre-processing block

✓ Pre-Processing:

Sign processing
Sorting the λ minimum magnitude

Sign(-Zmn)

Parity

Smn⁽ⁱ

FIFO

Zmn, n

|Zmn|, n

Min 0, n₀

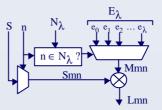
Min 1, n₁

 $Min 2, n_2$

 $\Omega_{\lambda}^{(i)}, N_{\lambda}^{(i)}$

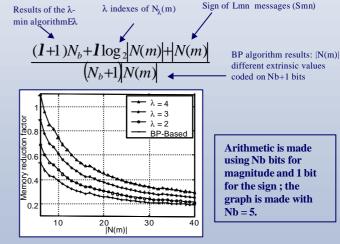


Generate each extrinsic information from the λ +1 messages computed by the λ -min algorithm.



Memory Reduction

The ratio between the memory used by the λ -min algorithm and the memory used by the BP algorithm for one parity check is given by:



For |N(m)|=20 and 1=3, up to 60 % of memory save compared to classical LDPC decoder.

