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DESIGN AND REALISATION OF A 100MHz SYNTHESIS CHAIN FROM AN X-BAND REFERENCE SIGNAL

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Abstract – LPMO has undertaken the building of a cryogenic sapphire oscillator with the support of the french Space and Metrology agencies (CNES and BNM). The aim of this project is to provide a reference oscillator presenting short frequency stability better than 5.10^{-14} in order to fulfill reference tests requirements for spacial and metrological applications [1]. The cryogenic oscillator can operate on different frequencies ranging from 8 to 13GHz depending on the sapphire resonator mode chosen as reference. The exact output signal frequency is not 'a priori' known with a great accuracy due to the large relative uncertainties (of the order of 10^{-4}) affecting the resonator frequencies theoretical determination. Then a special synthesis chain has to be designed in order to transfert the cryogenic oscillator performances to a reference signal whose frequency is fully compatible with most of Time and Frequency instrumentation. In this paper, we present the design, realization and preliminary tests of a synthesis chain generating a 100MHz signal from an X-band reference. The performances of the two realized prototypes will enable to transfert better than 5.10^{-14} short term frequency stability.

Keywords - Synthesis, 100MHz, X-band, DDS, Sampling Phase Detector

I. INTRODUCTION

Ultra-stable signals are now available in our laboratory from cryogenic sapphire oscillator in X-band [1]. This oscillator has been developed with the support of the *Centre National de la Recherche Spatiale* (CNES) and *Bureau National de Métrologie* (BNM) to provide an efficient tool for metrological measurements. Indeed the qualification tests of the new generation of on-board USO and synthesis systems requires the availability of a reference presenting frequency instabilities well below 5.10^{-14} on the short term.

Moreover the same reference are needed for the interrogating oscillator used in newly developed frequency standards based on cold atoms [2]. Our cryogenic oscillator is based on a 50 mm diameter high sapphire resonator operating on a Whispering Gallery Mode (WGM) near liquid Helium temperature. Several quasi transverse magnetic WGM separated by about 600MHz can be chosen as frequency reference.

Table I gives the frequency and the turn over temperatures of the most interesting modes of our sapphire resonator. The frequency stability of cryogenic oscillator is better than 2.10^{-14} for $\tau < 100s$.

TABLE I
FREQUENCIES, TURN-OVER TEMPERATURE, RANK OF THE USEFULL HARMONIC AND BEAT SIGNAL OF THE MOST INTERESTING MODES OF THE SAPPHIRE RESONATOR

| Mode designation | ν (GHz) | T_0 (K) | n | $\Delta\nu$ (MHz) |
|-----------------------|-------------|-----------|-----|-------------------|
| WGH _{13,0,0} | 9.747 | 7.33 | 98 | 53 |
| WGH _{14,0,0} | 10.353 | 7.66 | 104 | 47 |
| WGH _{15,0,0} | 10.959 | 6.61 | 110 | 41 |
| WGH _{16,0,0} | 11.565 | 6.42 | 116 | 35 |
| WGH _{17,0,0} | 12.170 | 6.60 | 122 | 30 |
| WGH _{18,0,0} | 12.774 | 6.58 | 128 | 26 |

The transfert of the cryogenic oscillator frequency stability to a 100MHz signal will be achieved by phase locking a 100MHz VCXO on a sapphire signal using the scheme given on figure 1.

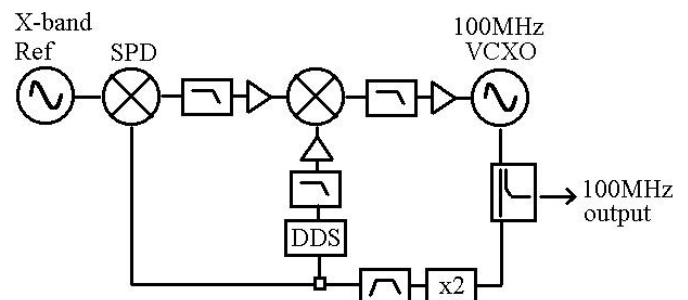


Fig. 1. Principle of the synthesis chain.

Sapphire and a high rank harmonic of the VCXO signals are compared in a Sampling Phase Detector (SPD) used as a Sampling Mixer, in order to produce a beat signal in the range 20-50MHz. In Table I, the rank n of the useful harmonic and the beat signal frequency are given. The PLL error signal is then obtained by mixing the beat note with the output of a Direct Digital Synthesis (DDS) referenced to a 200MHz signal coming from the VCXO frequency multiplied by 2, is needed to synthesize signal of 50MHz. Eventually, this error signal is supplied to the VCXO varicap to lock the loop. The use of a 48 bit DDS enables to achieve frequency of the order of 1.10^{-16} compatible with expected frequency accuracy of cold atoms frequency standards. Intrinsic phase noise of the synthesis chain components will limit the short term frequency stability of the 100MHz output signal. We present in this paper the measurement of individual components phase noise and the test of the overall system.

II. MULTIPLIER

The 100MHz signal from the VCXO is multiplied by two by this component. To obtain 200MHz from the 100MHz signal, we choose to send this signal through a 90°hybrid to the LO and RF of a mixer as schematized on figure 2. Actually, this configuration allow the lowest phase noise, compared to commercial multipliers and active multipliers using transistors. This comparizon has been made by the use of interferometric measurements at 100MHz [3].

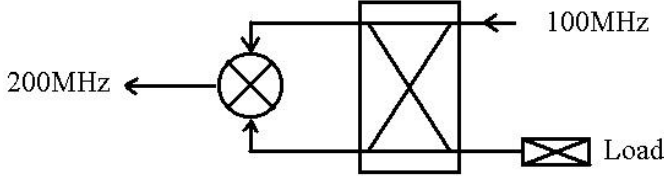


Fig. 2. Principle of the designed multiplier.

The 200MHz signal is used both to clock the DDS and to provide the LO signal of the SPD. The rejection of 100MHz pump signal and its harmonics 300 and 400MHz is better than 65 dBc. The phase noise power spectral density of two identical multipliers measured at 200MHz is given in figure 5 and Table II.

III. DIRECT DIGITAL SYNTHESIS

For Direct Digital Synthesis we use an AD9852 commercial model developed by *Analog Device Company* that uses a 48 bits phase accumulator, a 14 bits output converter and a working frequency that can be as higher as 300MHz. This model has been designed for numerical telecommunications applications.

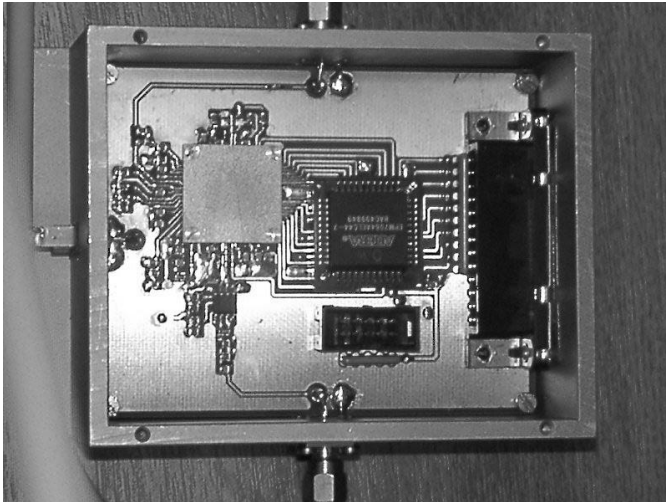


Fig. 3. AD9852 with EPLD and Parallel Port Connector.

There are several modes to be used, the fondamental one called single-tone is the most usefull for our application. It generate a sine signal by scrutation of a wave-table and digital-analogic conversion.

The frequency delivered by the DDS is :

$$F_{\text{signal}} = (p/2^{48}) \cdot F_{\text{ref}} \quad (1)$$

where p is the incrementation step of the phase accumulator defined as a 48 bits unsigned integer.

As 2^{48} is closed to $10^{14.5}$, the frequency resolution at 35MHz is closed to one microHertz.

We developed a card for the DDS with a driving module based on a Electrical Programable Logic Device (EPLD) that manage the parallel port from a personal computer. It allows the programmation of the DDS registers. In order to drain the heating because of the electrical consumption of the DDS, we put a copper thermal drain bridge that can be seen at the left on the picture. The 35MHz output signal power is only -5dBm. Then an amplifier stage has been placed at the DDS output with an anti-aliasing filter. The rejection of the filtering-amplification stage is greater than 40dBc on the harmonics of the 35MHz Intermediary Frequency (IF).

IV. SAMPLING MIXER

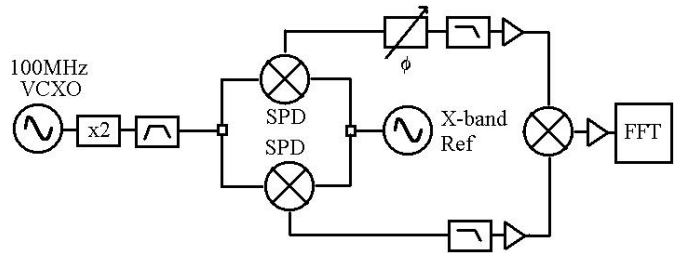


Fig. 4. Principle of the phase noise measurement of the Sampling Mixers.

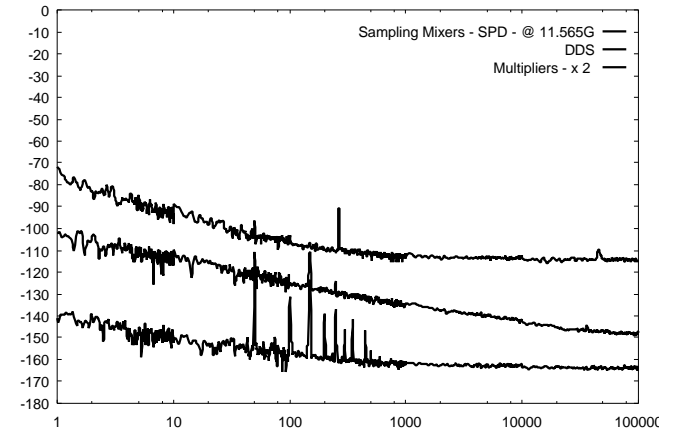


Fig. 5. Spectral density of phase noise S_{ϕ} (dB.rad²/Hz) versus Fourier frequencies (Hz) respectively from the top to the bottom for SPD, DDS and Multipliers.

This component, developed by *Avitronics* in South Africa, is protected by a radiator in order to operate at room temperature with an internal 36°C measured temperature for a 0dBm microwave input power. Spectral density of phase noise has been measured on two SPDs by rejecting the microwave signal delivered by a synthetizer splitted onto both SPDs, and LO pump signal was made of the

multiplication of the 100MHz from the VCXO. The 35MHz output signal phase noise of two SPD is represented in figure 5.

For one SPD, $\mathcal{L}(f) = -101 \text{ dBc/Hz}$ at 10Hz. Between 1Hz and 10Hz, the slope is a little bit higher than a $1/f$ slope. It could traduce the sensitivity of the SPD to the 11.5GHz 'RF' and 200MHz 'LO' signals. That is why we assume that the SPD introduce a noise $\mathcal{L}(f) = -91 \text{ dBc/Hz}$ at 1Hz.

V. NOISE PERFORMANCES

For each components of the synthesis chain, the performances are presented on table II in terms of spectral density of phase noise versus Fourier frequencies.

TABLE II

| SYNTHESIS CHAIN COMPONENT PHASE NOISE VERSUS FOURIER FREQUENCIES | | | | | | | |
|--|-------------------|---------------------|------|-------|-------|-------|--------|
| Noise (dBc/Hz) versus Fourier frequencies | Carrier frequency | Fourier frequencies | | | | | |
| | | 1Hz | 10Hz | 100Hz | 1kHz | 10kHz | 100kHz |
| Oscillator 11,5GHz | deduced at 100MHz | -117 | -147 | -177 | <-177 | <-177 | <-177 |
| VCXO | 100MHz | -75 | -106 | -135 | -161 | -176 | -177 |
| Multiplier 2x100MHz | 200MHz | -153 | -163 | -172 | -175 | -176 | -176 |
| DDS | 35MHz | -110 | -120 | -130 | -140 | -149 | -154,1 |
| Sampling Phase Detector | 35MHz | -91 | -101 | -113 | -120 | -121 | -121,5 |

VI. NOISE OF THE SYNTHETIZED SIGNAL AT 100MHz

From the contributions of each element of the synthesis chain, can be deduced the final noise level of the delivered signal at 100MHz. The noise level of the 100MHz synthesized signal can be estimated from the contributions of each preceding components. Assuming the phase lock loop in operation the error voltage fluctuations ΔV is given by:

$$\Delta V = K/p \cdot (\Delta \omega_i - \Delta \omega_j) \quad (2)$$

Where:

K is the sensitivity of the mixer in mV/rad

p is the Laplace's variable, and ω_i and ω_j are defined by:

$$\Delta \omega_i = \Delta \omega_{\text{Ref}} - n \cdot \Delta \omega_0 + \Delta \omega_{x2} \quad (3)$$

$$\Delta \omega_j = m \cdot \Delta \omega_s - m/2 \cdot \Delta \omega_{x2} + \Delta \omega_{\text{DDS}} \quad (4)$$

$\Delta \omega_s$, $\Delta \omega_{\text{Ref}}$ are the frequency fluctuations of the locked VCXO and the microwave reference respectively.

$\Delta \omega_{\text{DDS}}$, $\Delta \omega_{x2}$, $\Delta \omega_{\text{SPD}}$ are the frequency fluctuations introduced by the DDS, the multiplier by two, the sampling mixer, due to their intrinsic phase noise $\Delta \omega = 1/p \cdot \Delta \Phi$.

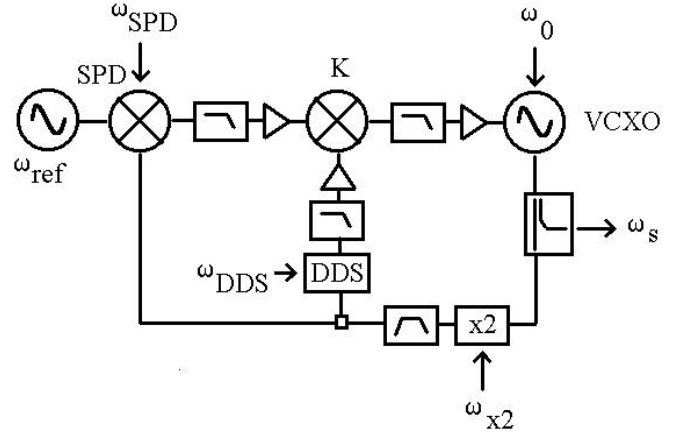


Fig. 6. Schematic representation.

- n defined in Table I

- m the ratio between the output frequency of the DDS and 100MHz

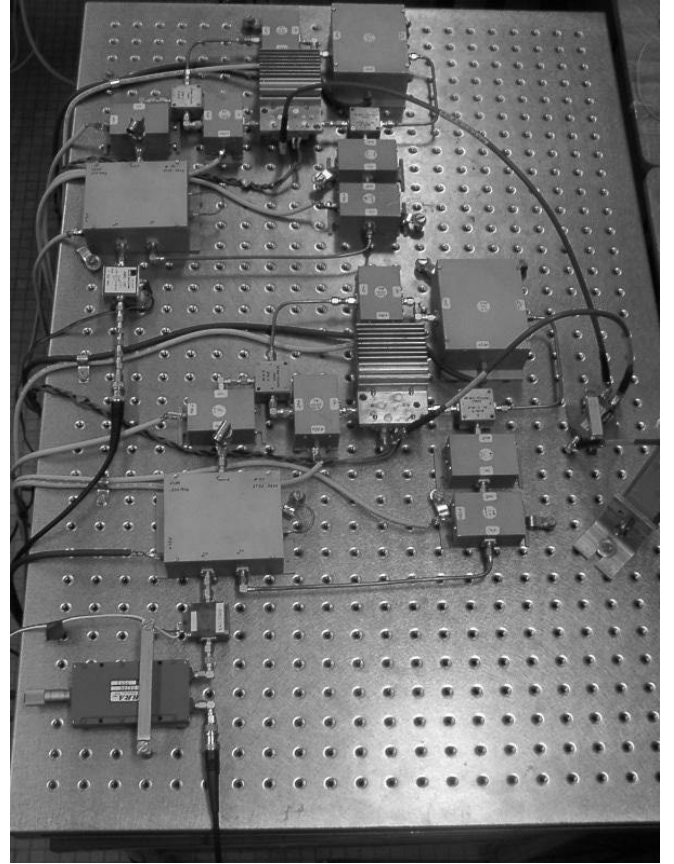


Fig. 7. The two synthesis chains

At the output of the VCXO, the signal is defined by:

$$\omega_s = \omega_0 + K_{\text{VCO}} \cdot \Delta V \quad (5)$$

Where K_{VCO} the VCXO tuning constant in Hz/V.

$$Sj_s = \left(\frac{4p^2 t^2}{1 + 4p^2 t^2} \right) Sj_0 + \left(\frac{1}{1 + 4p^2 t^2} \right) \frac{1}{n^2} (Sj_{ref} + Sj_{DDS} + Sj_{SPD} + 4 \cdot Sj_{x2}) \quad (6)$$

The graph illustrates the phase noise performance of various frequency sources. The y-axis represents the phase noise $L(f)$ in dBc, ranging from -60 to -170. The x-axis represents the frequency f in Hz, on a logarithmic scale from 0.1 to 10k. The curves show that the Locked VCXO has the lowest phase noise across the frequency range, while the DDS contribution is the highest at low frequencies and levels off at higher frequencies.

| f (Hz) | VCXO (dBc) | Locked VCXO (dBc) | sapphire (dBc) | SPD (dBc) | DDS contribution (dBc) |
|--------|------------|-------------------|----------------|-----------|------------------------|
| 0.1 | -60 | -88 | -92 | -125 | -155 |
| 1 | -75 | -105 | -115 | -135 | -165 |
| 10 | -95 | -135 | -145 | -145 | -160 |
| 100 | -125 | -150 | -155 | -155 | -160 |
| 1k | -155 | -155 | -160 | -160 | -160 |
| 10k | -170 | -170 | -170 | -170 | -160 |

Although different frequencies were tested in X-band, we only present here the results for a 11.5GHz signal for a 0dBm input power. The noise of the 100MHz output frequencies synthesized from the chains is given in the figure 10. For other input

[1] P.Y. Bourgeois, Y. Kersalé, N. Bazin, M. Chaubet and V. Giordano, *Cryogenic opened cavity sapphire resonator for ultra stable oscillator*, paper ELL 38056 accepted for publication in Electronics Letters, 2003.

[2] A. G. Mann, G. Santarelli, S. Chang, A. N; Luiten, Ph. Laurent, C. Salomon, D. G. Blair and A. Clairon, *A high stability atomic fountain clock using a cryogenic sapphire interrogation oscillator*, Proc. IEEE IFCS, Pasadena, CA, USA, 1998, pp. 13-17.

[3] E. Rubiola and V. Giordano, *Advanced interferometric phase and amplitude noise measurements*, Review of Scientific Instruments, Vol. 73, No 6, June 2002, pp. 2445-2457.