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Cofabrication of semiconducting and superconducting YBa $_2$ Cu $_3$ O $_{7-\delta}$ devices on (100) Si substrates

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We report the process technology for the modular integration of YBa₂Cu₃O_{7- δ} (YBCO) and *p*-type metal-oxide-semiconductor (*p*-MOS) devices on the same silicon substrate. Basic test structures consisting of single *p*-MOS field-effect transistors with a Pt-based metallization and YBCO bridges were fabricated. After completion of the *p*-MOS fabrication, highly *c*-axis-oriented YBCO films showing a critical temperature of 86 K were grown on a free silicon surface. The electrical characteristics at 77 K of the *p*-MOS transistors were comparable to those of this technology with Al metallization. This means that no fatal degradation was introduced into the *p*-MOS process by the YBCO one. The cofabrication on the same silicon substrate of devices using such disparate technologies as YBCO and MOS is a very promising starting point for a new generation of monolithic integrated circuits combining the advantages of oxide and semiconductor properties. © 2004 American Institute of Physics. [DOI: 10.1063/1.1805198]

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High-temperature superconductor (HTS) materials offer unique properties that are currently being exploited in various areas of superconductive electronics, such as passive microwave devices, superconducting quantum interference device (SQUID)-based systems, sensors, and digital circuits. The major progress that enabled materials such as YBa₂Cu₃O_{7- δ} (YBCO) to be used in useful devices was the ability to grow high quality films. Dedicated ceramic substrates such as SrTiO₃ or MgO were generally employed in order to achieve the film epitaxial growth.² Together with cooling issues, depositing YBCO films onto semiconductor substrates, and furthermore, combining YBCO devices with active semiconductor circuits without compromising the structure, chemistry, and intrinsic properties of either one of them, are among the main concerns for a future breakthrough of HTS applications. In addition to further miniaturization and cost reduction, the reduced distances between sensors and electronics prevent noise pickup from the environment and crosstalk between lines in the case of sensor multiplexing, thus leading to enhanced overall performance.³ In the present work, we only focus on the technological problems associated with the combination of YBCO and semiconductor components on the same silicon substrate.

There are many papers published on successful YBCO thin-film deposition on silicon substrate, even junctions, and SQUIDs. However, the limited efforts of the international scientific community have been devoted to the development of HTS superconductor/semiconductor integrated systems. Early after the HTS material discovery, novel circuit combinations were proposed. Active semiconductor and HTS devices have been fabricated on the same substrate by Burns *et al.* The fabrication process was based on complementary metal-oxide-semiconductor (CMOS) technology on siliconon-sapphire substrates. In that way, the HTS circuit composed of epitaxial YBCO and buffer layers necessary for the junction fabrication could be deposited on sapphire. Both the semiconductor and the superconductor devices were oper-

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ated separately at 77 K. To our knowledge, all other attempts concerned hybrid fabrication on separate chips. Application-specific integrated circuits operated at 77 K were developed by Seidel *et al.*⁸ in standard bipolar CMOS technology to create complete dc-SQUID electronics, and by Voisin *et al.*⁹ in standard CMOS technology to create all the readout circuits and the programmable bias current sources that are needed to drive a bolometer array.

One critical step towards monolithic integration is obviously to make the two technologies compatible, which means to ensure the fabrication of both technologies without degrading either of them. Silicon micromachining techniques have already been successfully adapted to the fabrication of membrane-type YBCO microbolometers. 10-12 Good superconducting properties are obtained for YBCO films if the correct stoichiometry and especially the optimal oxygen content are respected. In particular, high temperature (700-750 °C) and oxygen are required during deposition to form epitaxial films. Furthermore, restrictive conditions have to be respected after deposition mainly in order to prevent oxygen loss; namely, no high temperatures (>100 °C) in an air or vacuum environment and no (or reduced) contact with water, photoresist, developer, and most of the chemical products used in clean room processes. Additionally, introducing exotic materials such as YBCO in equipments used in a semiconductor foundry is forbidden in the viewpoint of process cleanliness. It was therefore decided that the semiconductor circuit should be fabricated first and, if possible, that the modifications of the semiconductor technology should be made after its standard fabrication (back-end modification).

Since they are fabricated on the same substrate as is YBCO, the semiconductor devices have to operate at cryogenic temperatures (around 90 K). We selected a simple academic p-MOS technology on (100) n-type Si substrate, which is a four-level mask technology and uses boron doping diffusion. Gate-oxide thickness and channel length are 75 nm and 5 to 30 μ m, respectively. Al(1% Si) is generally used for the one-level metallization layer, and we had to replace it

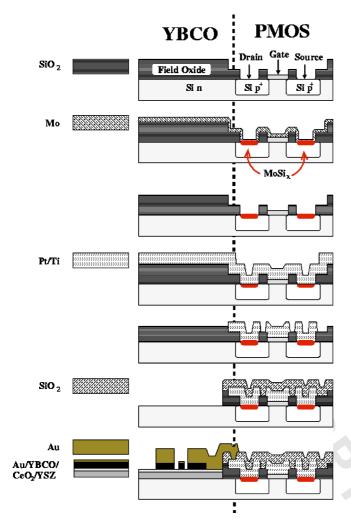


FIG. 1. Process flow for the cofabrication of p-MOS and YBCO devices.

since Al cannot stand annealing at temperatures above 525 $^{\circ}$ C, even with some barrier layers. 13

The complete fabrication sequence of integrated YBCO/p-MOS devices starting from p-MOS transistors without metallization is shown in Fig. 1. For the choice of the new metallization, one of our specific constraints was to achieve a good thermal stability and resistance against oxidization on both silicon (drain and source contacts) and silicon oxide (gate and interconnects). Based on previous measurements and bibliographic data about near-noble and refractory metal silicide formation, we decided to form the interconnection and gate metallizations using Pt/Ti bilayers (Ti promotes the adhesion of Pt on SiO₂) and the ohmic contacts onto silicon (drain and source terminals) using Pt/Ti bilayers on a molybdenum silicide (MoSi_x) thin layer. ¹⁴ A molybdenum layer was deposited first on the etched silicon contact windows and an annealing was performed for 60 min in vacuum at 600 °C [step (b) in Fig. 1]. The MoSi_x layer was selectively formed on the p^+ Si drain (or source) contacts but not on the SiO₂ layer (gate). Unreacted Mo could then be chemically etched [step (c) in Fig. 1], thus enabling the subsequent Pt/Ti layers to be directly deposited onto the SiO₂ areas (gate and interconnections) or onto the MoSi_r areas (drain and source).

At last, step (g) in Fig. 1 depicts the YBCO and buffer layer deposition and patterning; after that, part of the ${\rm SiO_2}$ layer was etched in a diluted NH₄F/HF solution on the area

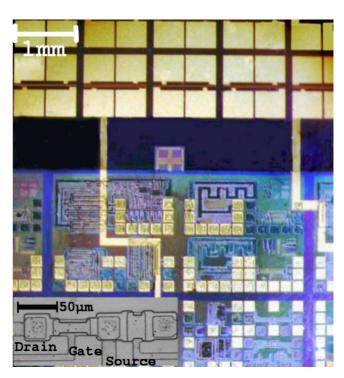


FIG. 2. Optical microscope photograph of a device containing p-MOS (bottom) and YBCO (top) devices on the same silicon substrate. Inset shows an optical photograph of a 30- μ m-wide 10- μ m-long transistor with a Pt-based metallization after O_2 annealing.

dedicated to YBCO. These layers were grown by KrF pulsed-laser deposition from stoichiometric targets onto the (100) Si substrates containing p-MOS transistors with the previously described Pt-based metallization. CeO₂/yttria -stabilized-zirconia (YSZ) buffer layers were used to avoid the strong interactions between Si and YBCO at the deposition temperature. $^{15\text{--}17}$ The $10~\text{mm}\times10~\text{mm}$ substrates were clamped in front of a resistive heater and radiantly heated from the backside. The laser radiation energy density was 2 J cm⁻² for YSZ and CeO₂ and 1.5 J cm⁻² for YBCO. A comprehensive x-ray diffraction study lead to the optimized deposition temperature of 700 °C for the three materials, and to the optimized O₂ pressures of 0.3 and 0.5 mbar for CeO₂ and YBCO, respectively. In the case of YSZ, the pressure was varied from 2×10^{-5} mbar at the early stage of growth to 10⁻⁴ mbar during the YSZ deposition. Right after deposition, a 700 mbar oxygen pressure was introduced in the deposition chamber and the films were cooled to ambient temperature at 20 °C/min including a 30 minute plateau at 500 °C. The typical layer thicknesses used in this study were 80, 10, and 230 nm for YBCO, CeO₂, and YSZ, respectively.

Figure 2 displays an optical microscope photograph of a device containing p-MOS (bottom) and YBCO (top) devices on the same silicon substrate. Gold lines between the two area can be seen, but they are not operational since the devices were tested separately. The inset in Fig. 2 shows a typical optical photograph of a 30- μ m-wide 10- μ m-long transistor with a Pt-based metallization after O_2 annealing. After YBCO deposition, the sheet resistivity of the Pt-based multilayers was measured on a 50- μ m-wide and 3260- μ m-long line. As described in Ref. 14, the sheet resistances ($R_{\rm sheet}$) of unpatterned Pt/Ti on SiO₂/Si did not change after annealing in O_2 (0.5 mbar) at 700 °C for 1 h, roughly reproducing the deposition conditions of YBCO. The specific contact resistance defined as ρ_c = R_c ×A, where A is the contact area

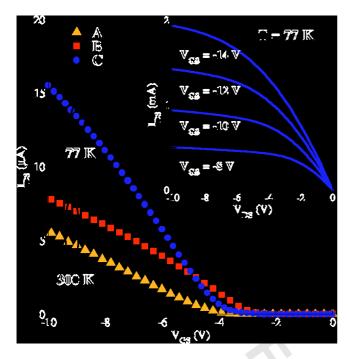


FIG. 3. $I_{\rm DS}(V_{\rm GS})$ characteristics at $V_{\rm DS}$ =-0.1 V of a 30- μ m-wide 10- μ mlong transistor with the Pt-based metallization as deposited (curve A) and after the YBCO deposition sequence at 300 K (curve B), and at 77 K (curve C). Inset shows the $I_{DS}(V_{DS})$ characteristics after YBCO deposition at 77 K.

[cm²], was measured on a chain of 14 contacts in series. The extracted sheet resistivity and specific contact resistivity were 0.45 Ω /sq and 2×10⁻⁴ Ω cm², respectively. The drain current (I_{DS}) versus gate voltage (V_{GS}) and versus drainsource voltage ($V_{\rm DS}$) characteristics of a 30- μ m-wide 10- μ mlong transistor are presented in Fig. 3 at 300 and 77 K. Before YBCO deposition, the threshold voltage V_T was -4 V and the transconductance g_m was 7.4×10^{-5} A V⁻¹ (at 300 K, $V_{\rm DS} = -5$ V and $(V_{\rm GS} - V_T) = -5$ V). After YBCO deposition, these values improved to $V_T = -3$ V and $g_m = 7.9$ $\times 10^{-5}$ A V⁻¹. Finally the transistors were tested at 77 K $(V_T = -4 \text{ V} \text{ and } g_m = 19.1 \times 10^{-5} \text{ A V}^{-1})$. All these values are close to those we currently obtained for transistors of same technology with aluminum contacts.

The x-ray diffraction study showed that the YBCO films were highly c-axis oriented. The resistance versus temperature characteristics of YBCO films deposited onto buffered-Si substrates containing p-MOS transistors with Ptbased metallization, as described previously, and onto a standard buffered-Si substrate for comparison are shown in Fig. 4. The critical temperature and the maximum (1/R) $\times (dR/dT)$ values of the films were about 86 K and 0.83 K⁻¹, respectively, which is slightly smaller than the values we typically obtain on standard (100) Si substrates (88 K and 1.26 K⁻¹). Despite this slight degradation of performances such YBCO film is still very useful for bolometric applications.

This letter reports the cofabrication of a superconducting YBCO film with critical temperature of 86 K and an active semiconductor device on the same silicon substrate. This opens the route for the fabrication of matrices of fully integrated monolithic semiconductor amplifier/superconductor YBCO microbolometers. This process has now to be trans-

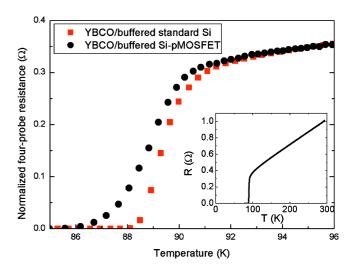


FIG. 4. Normalized resistance (with respect to the value at 300 K) versus temperature characteristics of 80-nm-thick YBCO films deposited on CeO₂/YSZ buffered standard Si or Si containing the *p*-MOS devices. Inset shows the R(T) characteristics in the 0–300 K range.

ferred to a more advanced semiconductor technology in which dedicated bolometer readout circuits could be designed, and it could be enlarged to all other oxide-based technologies such as ferroelectrics and manganites.

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