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## IMPLICATIONS OF THE INTERFACE EFFECTS IN THE NORMALLY-OFF TYPE GaAs MESFETs

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**Résumé.** — On compare, pour les types normally-on et normally-off, l'évolution des caractéristiques  $I-V$  de MESFET-GaAs de structure plane à canal long sous l'effet d'une polarisation du substrat. On montre que l'interprétation des résultats nécessite de tenir compte, en plus de la zone de charge d'espace Schottky, d'une zone déserte à l'interface canal-substrat ainsi qu'à la surface de l'espace source-grille. Cette dernière, qui n'a qu'une influence mineure pour le type normally-on, dégrade fortement le courant du FET normally-off et limite les tensions de seuil positives réalisables. D'autre part, le confinement des porteurs entre deux charges d'espace conduit à une description théorique simple du canal hors neutralité, ce qui permet un contrôle précis de la tension de seuil, même pour les couches très minces.

**Abstract.** — The variations of  $I-V$  characteristics under substrate bias are compared for normally-on and normally-off type planar GaAs-MESFETs with long-channel. The experimental results are interpreted by superimposing to the Schottky gate space-charge region both a depleted layer at the channel-substrate interface and a depleted surface region between source and gate. This last one is only of minor influence on normally-on characteristics, but strongly reduces the normally-off current and limits the achievable positive threshold voltages. On the other hand, the carrier confinement between two space-charge layers leads to a simple theoretical model for the no-neutral channel, allowing an accurate threshold voltage control even for very thin layers.

1. **Introduction.** — It has been shown recently [1, 2] that the normally-off type GaAs-MESFETs offer potential for very low-power high-speed logic circuits. Though such an approach appears as very promising, the presently measured performance can be looked as limited by subsidiary interface effects whose reduction will further allow a substantial performance improvement, especially concerning the speed. Directed toward this goal, it is the purpose of this paper to investigate the role played by these interface effects both in the characteristics prediction and in the operation of the planar normally-off type GaAs-MESFET. For a best understanding, the analysis will be performed by comparing with the more usual case of normally-on transistors.

2. **Device parameters.** — The experimental support of this work was provided by MESFETs whose size was chosen very large (gate length  $L = 50 \mu\text{m}$ , gate width  $Z = 300 \mu\text{m}$ ) in order to minimize the two-dimensional and hot-carrier effects, and to allow accurate gate capacitance measurements even in the pinchoff region. These devices were fabricated on vapor phase deposited GaAs layers onto Cr-doped GaAs semi-insulating substrates. The epitaxy was performed using either a standard  $\text{AsCl}_3/\text{Ga}$  process or a low-pressure  $\text{Ga}(\text{CH}_3)_3$  cracking method. Several wafers with a  $3\text{-}5 \mu\text{m}$  high-purity buffer layer were also included in this study.

As shown in figure 1, the saturated current of a long-channel transistor can be very well fitted by the relation :

$$I_{DS} = (Z/L) \gamma (V_{GS} - V_T)^2 \quad (1)$$

which defines two important parameters of the MESFET :

(i) the threshold voltage  $V_T$ , ranging from about  $-3 \text{ V}$  (normally-on) to  $+0.1 \text{ V}$  (normally-off MESFET),

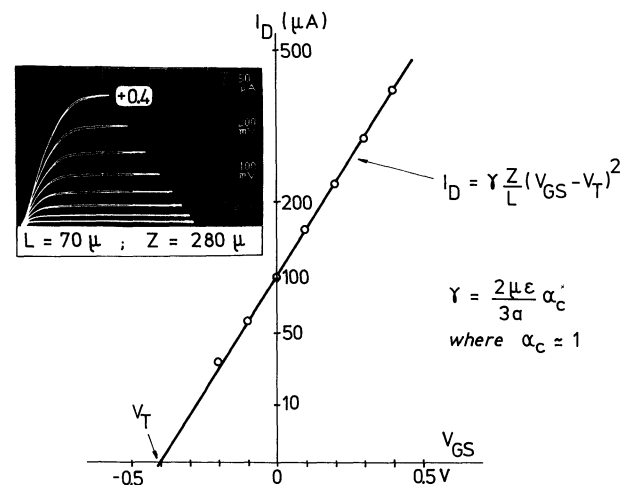


FIG. 1. — Experimental relation between saturated drain current and gate-source voltage for a long-channel epitaxial GaAs-MESFET.

(ii) the current control factor  $\gamma$ , depending on the doping profile, mobility, gate length, and gate-source parasitic resistance  $R_{SG}$ .

Notice that equation (1) remains approximatively valid even for short-channel MESFETs and thus appears as a convenient relation to describe the overall characteristic of the transistor. For integrated circuit applications, the parameter  $\gamma$  must be looked as directly governing the switching speed, because it determines the available current for charging/discharging the overall drain-node capacitance.

3. The  $\gamma$ - $V_T$  plot. — 3.1 THEORY. — In the ideal case where the channel is uniformly doped (concentration  $N$ , thickness  $a$ ) and  $R_{SG}$  is neglected, the parameters  $V_T$  and  $\gamma$  can be expressed by :

$$V_T = V_{bi} - V_P = V_{bi} - \frac{qNa^2}{2\epsilon} \quad (2)$$

$$\gamma(R_{GS} = 0) = \gamma^* = \frac{2\epsilon\mu}{3a} \alpha_c \quad (3)$$

where :  $V_P$  : pinchoff voltage;  $V_{bi}$  : gate-channel built-in voltage (typical value : 0.7 V);  $\gamma^*$  : intrinsic current control factor.

The current reduction factor  $\alpha_c$  in equation (3) results from the drift velocity saturation at the critical field  $E_c$ . In the one-dimensional approximation,  $\alpha_c$  can be deduced as a function of  $L$  and  $V_P$  from a model similar to that of reference [3] by the cubic equation :

$$2(\alpha_c/\lambda)^3 - 3(\alpha_c/\lambda)^2 + 1 - \alpha_c = 0 \quad (4)$$

$$\lambda = 3LE_c/V_P. \quad (5)$$

In the actual case where  $R_{SG}$  must be taken into account, the extrinsic factor  $\gamma$  is derived by identifying the drain current :

$$I_D = \gamma^*(Z/L) (V_{GS} - V_T - R_{SG} I_D)^2 \quad (6)$$

with equation (1) for  $V_{GS} = V_{bi}$ .

In most practical cases, GaAs-MESFETs are fabricated by using a channel concentration as constant as possible and even chosen within a narrow range (typically  $5 \times 10^{16}$  to  $1 \times 10^{17} \text{ cm}^{-3}$ ). This being so, the channel thickness is deduced, as a technological parameter, from the expected  $V_T$ . Thus it appears from equations (2) and (3) that plotting  $\gamma$  versus  $V_T$  at constant concentration is a convenient characteristic for a given transistor, since this plot must be seen as the locus of MESFET parameters when varying the channel thickness. It will be shown later that the  $\gamma$ - $V_T$  plot is also convenient to discuss interface effects.

3.2 ANALYSIS OF EXPERIMENTAL RESULTS. — All the studied transistors showed a variation both for DC voltage-current and for Schottky-gate voltage-capacitance characteristics when the semi-insulating substrate was biased negatively with respect to the source contact. This substrate bias effect, whose sensitivity strongly depends on the peculiar epi-layer, always leads to shift  $V_T$  toward positive values. Adversely, the  $\gamma$  variation differs for normally-on and normally-off transistors.

In figure 2, the typical curve described in the  $\gamma$ - $V_T$  plot under substrate bias effect for a normally-on MESFET is shown. It appears that  $\gamma$  increases slowly with  $V_T$  and that very high substrate voltages are needed to modify the MESFET parameter substantially. With usual voltages encountered in ICs, the substrate bias effect thus appears only of minor consequence. In figure 3 conversely, the same curve for a nearly normally-off transistor is shown. It can be seen that the substrate bias effect is now responsible for a sharp decrease of  $\gamma$  when  $V_T$  is raising about zero.

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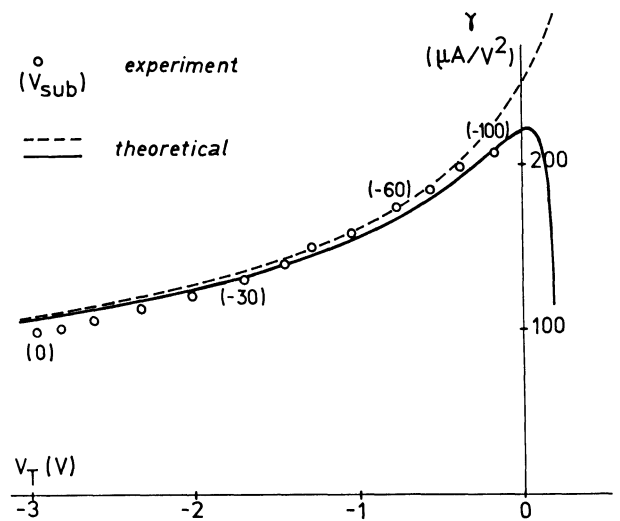


FIG. 2. —  $\gamma$  versus  $V_T$  plot for a normally-on GaAs-MESFET ( $L = 50 \mu\text{m}$ ,  $Z = 300 \mu\text{m}$ ). Dots : experimental results obtained by varying substrate-source voltage from 0 to  $-100$  V. Curves : calculated characteristics at variable channel thickness, with :

$$N = 5 \times 10^{16} \text{ cm}^{-3}, \quad \mu = 5000 \text{ cm}^2/\text{V.s}, \quad L_{SG} = 2 \mu\text{m},$$

$r_c = 10^{-5} \Omega \cdot \text{cm}^2$ ,  $\psi_s = 0$  (dashed curve) and  $\psi_s = 0.5$  V (solid line).

The dashed curve in figure 2 gives the theoretical  $\gamma$ - $V_T$  characteristic as deduced from theory of section 3.1 when the usual expression, for  $R_{SG}$

$$R_{SG} = (R_{\square} \cdot L_{SG} + \sqrt{R_{\square} \cdot r_c})/Z \quad (7)$$

was used and where :  $R_{\square} = 1/q\mu Na$  : sheet resistance of the N type-layer;  $L_{SG}$  : source to gate spacing;  $r_c$  : specific contact resistance of the source ohmic contact (typical values  $r_c = 10^{-6}$  to  $10^{-5} \Omega \cdot \text{cm}^2$ ).

It can be seen that, apart from a small deviation at lowest substrate voltages the agreement with the experimental results is excellent. Thus, it may be stated that the substrate bias effect can be described as

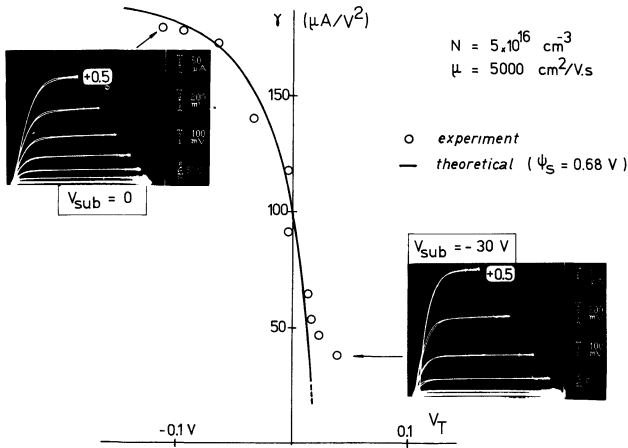


FIG. 3. —  $\gamma$  versus  $V_T$  plot and drain current characteristics for a nearly normally-off GaAs-MESFET ( $L = 50 \mu\text{m}$ ,  $Z = 300 \mu\text{m}$ ). Dots : experimental results obtained by varying substrate-source voltage from 0 to  $-30 \text{ V}$ . Curve : calculated characteristic at variable channel thickness with the same data as figure 2 except  $\psi_s = 0.68 \text{ V}$ .

a channel thickness modulation whose physical origin must be inquired at the channel-substrate interface. This result is consistent with other experimental evidences [4, 5, 6] leading to conclude that the channel is limited towards the substrate by a depleted region due to defects at the metallurgical interface.

Oppositely, a comparison between the strong raising of dashed curve of figure 2 in the normally-off region and the experimental results of figure 3 shows a severe discrepancy. To explain this, it must be remembered that eq. (7) suppose a flat-band condition at the GaAs surface in the source-gate interval. If surface-states are present, they would lead to a depleted region at the surface with a band bending  $\psi_s$ , and eq. (7) must be replaced by :

$$R_{SG} = \frac{1}{Z} \left[ \frac{R_{\square} \cdot L_{SG}}{1 - \sqrt{\psi_s/V_P}} + \sqrt{R_{\square} \cdot r_c} \right]. \quad (8)$$

This equation leads to the theoretical solid lines of figures 2 and 3, which exhibit a decaying  $\gamma$  for  $V_T = V_{bi} - \psi_s$ . Agreement between theory and experiment can be looked as proving that such a depleted surface region is present in the actual normally-off devices.

As a conclusion, figure 4 schematically summarizes the subsidiary depleted regions to take into account in order to explain the DC voltage-current characteristics of the planar GaAs-MESFET in a wide range for  $V_T$  including the normally-off case.

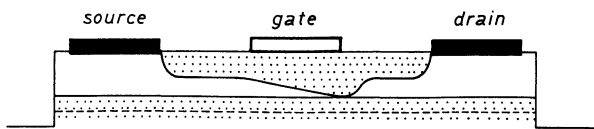


FIG. 4. — Schematic cross section of a planar GaAs-MESFET showing the depleted region as concluded by this work.

**4. Practical consequences.** — 4.1 CONTROL OF  $V_T$  FOR A NORMALLY-OFF MESFET. — The fabrication of GaAs-MESFET ICs requires a close control for  $V_T$ , especially with normally-off transistors for which a maximum deviation of about  $100 \text{ mV} = 4 kT/q$  is needed. This can be achieved practically by controlling the epi-layer thickness whose value can be accurately adjusted by anodic oxidation. However, such a method supposes that the initial characteristics of the active layer are known.

In figure 5, the carrier concentration profile deduced as usually from Schottky C-V data both for a normally-on and a normally-off epi-layer is shown. It is obvious that no sufficient information can be deduced from this last profile. Thus, it is more convenient to pre-determine  $V_T$  directly from the C-V plot. However, for very thin layers, only a small portion of this curve is available, corresponding to a complicated situation where the quasi-neutrality approximation is no longer valid.

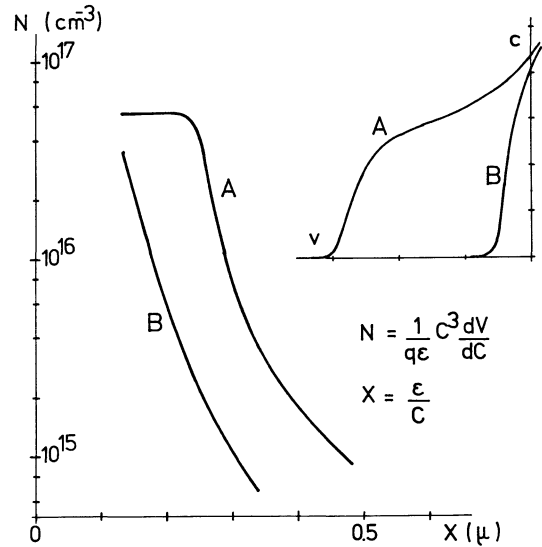


FIG. 5. — Schottky C-V characteristics and deduced carrier concentration profiles for a normally-on (curves A) and a normally-off type (curves B) epilayer.

Knowing that the channel carriers are confined between two interacting space charge layers, the potential equation across the channel can be solved numerically allowing to deduce the net positive charge under the gate (Fig. 6) and the Schottky-gate C-V characteristic, even around no-neutral pinchoff conditions. As shown in figure 7, fitting the theoretical C-V curve with experimental data allows to determine the characteristic parameters of the epi-layer, especially in the normally-off case where usual methods cannot be applied.

4.2 SURFACE CHARACTERIZATION OF EXTRINSIC ZONES. — The effective surface band bending between the contacts can be easily deduced from the  $V_T$  value

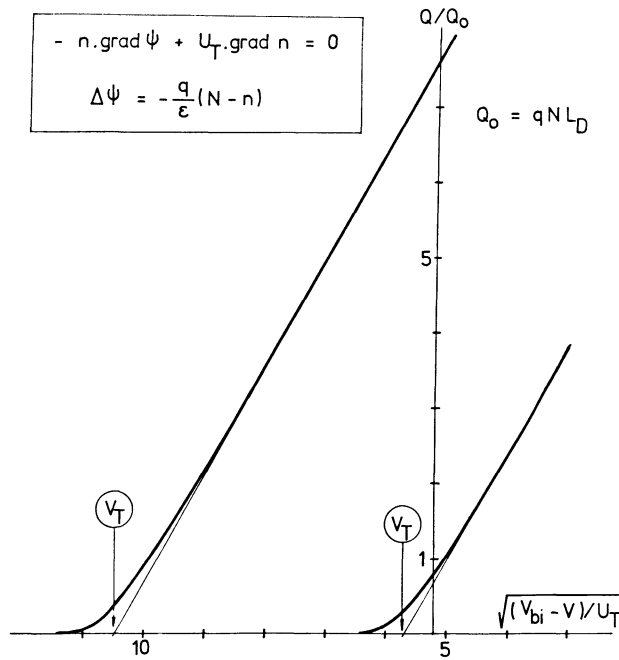


FIG. 6. — Numerically computed relation between the net positive charge under the gate and the gate-channel potential.

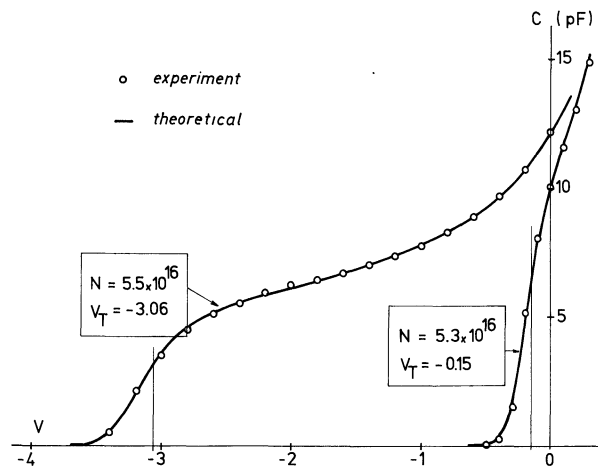


FIG. 7. — Experimental (dots) and fitted theoretical (solid curves) Schottky C-V characteristics both for a normally-on and a nearly normally-off epi-layer. Active layers parameters as deduced from the fit are indicated.

at which  $\gamma$  vanishes. As an example, in figure 8 the  $\gamma$ - $V_T$  distribution for a set of normally-off type MESFETs issued from the same wafer and measured at various substrate potentials (0 to  $-10$  V) is shown. The various points refer either to a passivated (sputtered  $\text{SiO}_2$ ) or free surface. They are well fitted by a theoretical curve corresponding to an effective surface band bending of  $0.56$  V. Subsidiarily, it can be seen

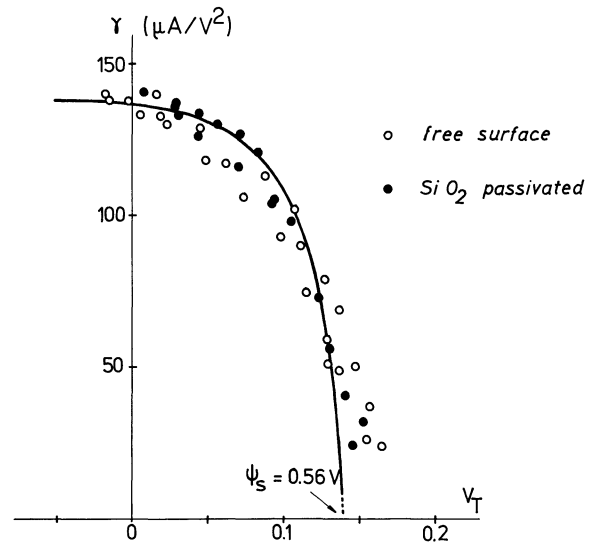


FIG. 8. — Determination of the effective surface band bending between the contacts with application to the study of passivation.

that the passivation is not efficient to eliminate the surface depletion.

**5. Conclusions.** — It has been demonstrated that a proper description of planar GaAs-MESFET DC-characteristics over a wide range of threshold voltages including the normally-off type needs to superimpose to the gate space-charge region a depleted zone both at the surface between the contacts and at the epilayer-substrate interface.

The epilayer-substrate depleted region is responsible for a substrate bias effect which can be seen as an effective channel thickness modulation. It must be taken into consideration when interpreting carrier concentration profiles across the channel. On the other hand, two dimensional numerical computations show that the existence of an interfacial depleted zone strongly influences the behavior of the trapped Gunn domain in the FET channel and thereby the saturation characteristics of the transistor [7].

The surface depletion between source and gate, which is only of minor consequence for normally-on MESFET, strongly influences the normally-off characteristics. Looking to the ICs applications, the surface band bending leads to the following disadvantages : (i) existence of a maximum achievable positive threshold voltage, (ii) reduced fabrication yield by spreading the variations of the electrical characteristics, (iii) decrease of the switching speed. Drastic improvement in normally-off performance and fabrication yield can be obtained by using a transistor design and a fabrication process taking the previous conclusions into account. Especially, a surface over-doping of extrinsic zones and/or a notched channel structure can be looked as beneficial for normally-off MESFET IC technology.

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